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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,842	11/15/2000	Sudhakar Muddu	062986.0221 (1071.00)	4796

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Baker Botts L.L.P.
2001 Ross Avenue
Dallas, TX 75201-2980

EXAMINER	
PALADINI, ALBERT WILLIAM	
ART UNIT	**PAPER NUMBER**
2125	4

DATE MAILED: 04/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No. 09/713,842	Applicant(s) MUDDU, SUDHAKAR	
	Examiner Albert W Paladini	Art Unit 2125	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not use the classic definition of node, which is a single point in an electrical circuit through which electrical current flows. Instead the definition of node is provided on lines 14-15 of page 6, which states, "Nodes 106 represent elements such as transistors of an integrated circuit." Then lines 21-25 on page 6 state "Response describes the behavior of an interconnect in accordance with an applied signal, for example, the response of interconnect 102d describe the behavior at node B 106e in response to a signal applied at node A 106d." The description on page 6-8 describe obtaining a transfer function H(s) using electrical parameters such as the inductance, resistance, and capacitance of the interconnect, as summarized on the bottom of page 7. This analysis does not take into account the electrical characteristics and transfer functions of the nodes themselves. For example, if node 106d A is a transistor, then interconnect 102c is connected to one terminal of transistor 106d A, and

interconnect 102d is connected to a second terminal of transistor 106d A. There is thus an impedance and transfer function between the first and second terminals of transistor 106d A. The analysis on pages 6-8 is incomplete because it ignores the transfer functions of circuit elements 106 of the integrated circuits and consider only the transfer functions of the interconnects 102. The circuit element 106d a is treated as if it were a single point, which would be consistent with the classical definition of node. Since it has been established that elements 106 are circuit elements, the analysis is incomplete and therefore inaccurate. Since every node 106 is a circuit element, it has more than one terminal, and therefore an impedance or transfer function between terminals. The transfer function of each node 106 has not been considered in the analysis.

Appropriate correction and clarification is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pillage (5379231).

Pillage discloses a method and apparatus for simulation a micro electric interconnect circuit. Pillage teaches the incorporation of inductance in obtaining the transfer function in column 2, lines 4-12 where he states "Even inductance effects, which are evident for boards and multichip modules which comprise microelectronic systems, may also be important for modeling the integrated circuit packaging or chip-to-package interface.

Accordingly, a complete circuit simulation of an integrated circuit must now account for the resistive, inductive and capacitive effects of the interconnect paths in addition to simulating the effect of the active devices on the integrated circuit." The poles of the transfer function are discussed in column 2, lines 29-45, where he states, "Described is an Asymptotic Waveform Evaluation (AWE) methodology to provide a generalized approach to linear resistor-inductor-capacitor (RLC) circuit response approximations. AWE is a general method for computing any number of moments for any linear circuit. Using the method, a qth order approximation to the actual circuit response can be obtained by computing 2 q moments of the circuit and matching these moments to the circuit's impulse response. The moments, in their simplest interpretation, represent the coefficients of the s-terms in the Taylor series expansion of the homogenous circuit response. Once the desired number of moments are found, they may be mapped to the dominant poles and corresponding residues. Once the poles and residues of the approximate response are found, the time domain response of the interconnect circuit may be determined." The use of the aforementioned parameters to obtain interconnect delays is taught in column 8, lines 3-6 where he states "The AWE methodology represents a qth order extension of the first-order Elmore delay approximation and can be used to predict a transient waveform at any circuit node."

Pillage does not explicitly discuss the order of the analysis to obtain the delay as recited in the claims. It would have been obvious to one of ordinary skill in circuit analysis, that an analysis starts with the estimation of circuit parameters such as inductance or resistance, uses these elements in the selected circuit configuration to obtain impedance and transfer functions, and uses the transfer functions to determine the circuits operation as a function of time when signals are applied.

Relevant Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rohrer (5313398) discloses a method and apparatus for simulating a microelectronic circuit where the linear and non-linear elements are analyzed to obtain poles resulting in a time domain simulation of the circuit.

Kashyap (6496960) discloses a method for determining a driving point model utilizing a reduced order circuit for determining a delay of a gate driving an interconnect having resistive, capacitive, and inductive elements.

Ismail (6460165) discloses a model for simulation an RLC tree structured VLSI interconnects by obtaining transfer functions and determining the poles and zeros to obtain transient responses.

6. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (703) 308-2005. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (703) 308-0538. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

April 1, 2004

Albert W. Paladini
Primary Examiner
Art Unit 2125